# Extending the Bandwidth Performance of Heterojunction Bipolar Transistor-Based Distributed Amplifiers

Kevin W. Kobayashi, *Member, IEEE*, Liem T. Tran, *Member, IEEE*, John C. Cowles, *Member, IEEE*, Thomas Ray Block, Aaron K. Oki, *Member, IEEE*, and Dwight C. Streit, *Senior Member, IEEE*

***Abstract*—An InAlAs/InGaAs-InP HBT CPW distributed amplifier (DA) with a 2–30 GHz 1-dB bandwidth has been demonstrated which benchmarks the widest bandwidth reported for an HBT DA. The DA combines a 100 GHz fmax and 60 GHz fT HBT technology with a cascode coplanar waveguide DA topology to achieve this record bandwidth. The cascode gain cell offers 5–7 dB more available gain (MAG) than a common-emitter, and is used to extend the amplifier's upper frequency performance. A coplanar waveguide design environment is used to simplify the modeling and fabrication, as well as to reduce the size of the amplifier. Novel active load terminations for extending the DA's lower frequency response were separately demonstrated. The active loads are capable of extending the lower bandwidth performance by two decades resulting in performance below 45 MHz. This work explores both design techniques and technology capability which can be applied to other distributively matched HBT circuits such as active baluns for mixers, active combiners/dividers, and low dc power-broadband amplifiers.**

## I. Introduction

MMIC distributed amplifier design has been applied to wideband power amplifiers and active power combiners/dividers [1], [2], wideband switches [3], [4], active baluns for mixers [5], [6], and wideband amplifiers for ultra high speed electro-optical communication [7], [8]. All of these MMIC demonstrations have been based on either MESFET or HEMT technology. Recently due to the advancement of AlGaAs/GaAs HBT device and MMIC design technology, HBT distributed amplifiers with wide bandwidth performance have been demonstrated [9]–[12].

The first GaAs HBT distributed amplifier reported achieved 11 dB gain and a 6.5 GHz bandwidth (BW) [9], while a record gain-bandwidth product of 84 GHz was achieved for a GaAs HBT DA by employing input and output loss-compensation techniques [11]. Until now, the widest bandwidth (1-dB) recorded for an HBT DA was 22.5 GHz and had a nominal gain of 10 dB [10]. This performance was accomplished by utilizing a 2 × 3 matrix distributed amplifier topology and employed an exponentially graded base doping profile to reduce the HBT device input capacitance. In the work presented in this article, we extend the upper 1-dB band edge response to 30 GHz by employing high performance InAlAs/InGaAs-InP HBT cascode devices in a coplanar waveguide distributed amplifier design. While an InAlAs/InGaAs-InP HBT cascode direct-coupled amplifier with a 33 GHz 3-dB bandwidth has been previously demonstrated [13], this amplifier was limited to a practical bandwidth of 16 GHz due to its poor input and output return-loss. On the other hand, the HBT cascode distributed amplifier design can achieve good broadband return-loss which is typically >13 dB across the full band.

In a separate demonstration, the low frequency response of the HBT cascode DA was extended below 45 MHz using novel HBT active load transmission line terminations. Combined with the 30 GHz upper frequency capability, a baseband to millimeter-wave frequency HBT actively terminated DA design topology results which can accommodate next generation ultra high data rate electro-optical communications at millimeter-wave frequencies.

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The authors are with TRW Electronics Systems and Technology Division, Redondo Beach, CA 90278 USA.

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## II. InAlAs/InGaAs HBT Technology

A similar 1-$\mu$m fully self-aligned InAlAs/InGaAs HBT process has previously been described in detail [14] along with several MMIC demonstrations [15], [16], [17], [18], [19]. The InAlAs/InGaAs HBT device structures are grown using solid source molecular beam epitaxy. Be and Si are used as $p$- and $n$-type dopants for the base and emitter/collector, respectively. The base-collector epitaxial structure consists of a base thickness of 800 Å uniformly doped to $3 \times 10^{19}$ cm$^{-3}$, a 7000 Å thick $n$-type collector lightly doped to $1 \times 10^{16}$ cm$^{-3}$, and an $N^+$ sub-collector doped to $2 \times 10^{19}$ cm$^{-3}$. The emitter structure incorporates an InGaAs/InAlAs cap which is heavily doped for good emitter contact. The base-emitter junction consists of a compositionally graded quarternary layer of $In_{1-x-y}Ga_xAl_yAs$. Compositional base-emitter grading is used to achieve uniformly consistent dc beta and $V_{be}$ matching between devices, as well as for producing consistently repeatable device rf performance. The HBT dc beta across the wafers are typically 20 at a $J_c = 10$ kA/cm$^2$. The breakdown voltage $BV_{ceo}$ is $\approx$ 11 V and the $BV_{cbo}$ is $\approx$ 13 V.

A high performance fully self-aligned 1-$\mu$m emitter width process is used to produce HBT's with typical $f_T$ and $f_{max}$ (from MAG) of $\approx$ 60 GHz and 100 GHz, respectively. These numbers were achieved from a 1 × 10 $\mu$m$^2$ quad-emitter

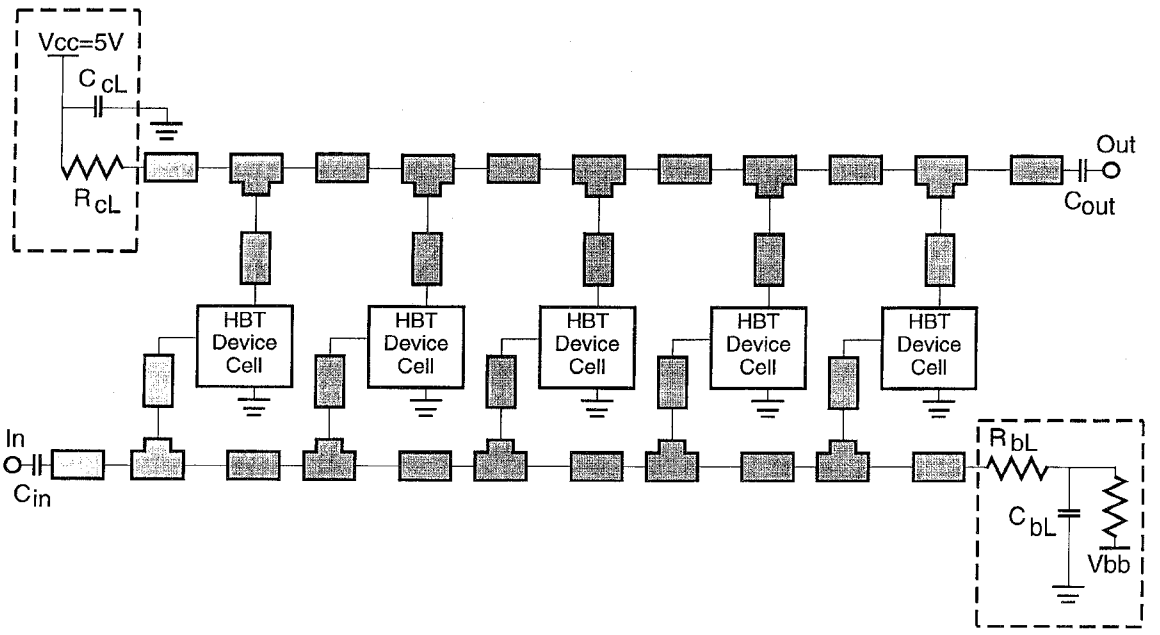



Fig. 1. Design topology of the five-section CPW HBT cascode DA.

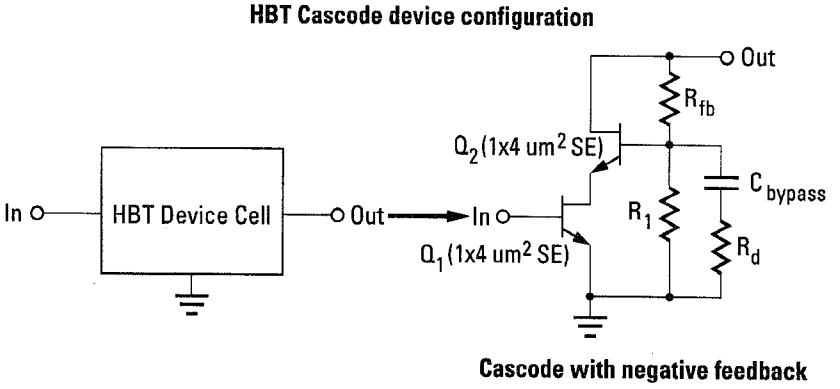


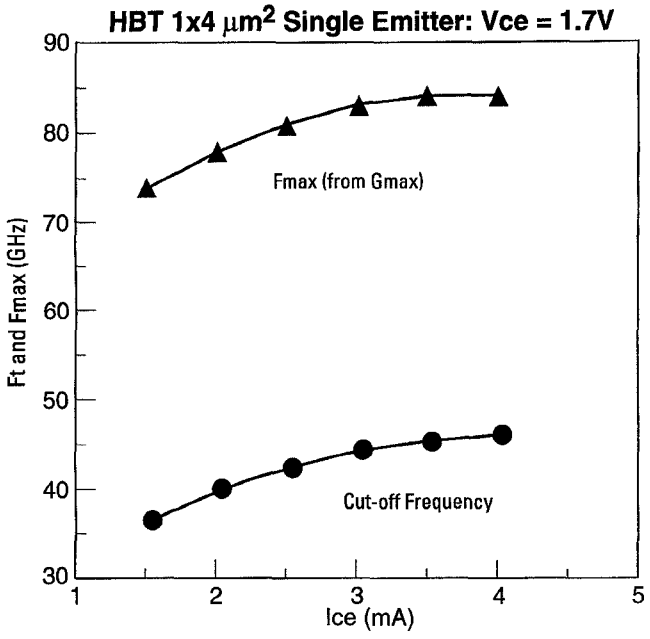

Fig. 2. HBT cascode gain cell.

HBT biased at a current density of $J_c = 120$ kA/cm$^2$ and a $V_{ce} = 2.0$ V.

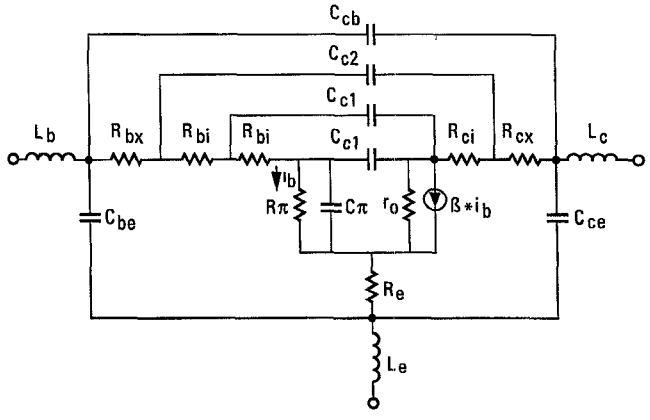
## III. CPW HBT Cascode Distributed Amplifier Design

The design schematic of a five-section CPW HBT cascode DA is given in Fig. 1. A CPW design environment was used because it offers smaller chip size implementation, lower parasitic ground inductance, and easier manufacturability because backside vias are not required. In addition, a CPW design environment can minimize interline coupling between transmission lines and proximity effects which simplifies the circuit modeling at millimeter-wave. This last advantage is especially attractive for millimeter-wave HBT DA's because the small inductive line lengths normally required to construct a distributive network with the HBT's high input capacitance are sensitive to the close proximity of backside vias and other microstrip components. Also, the high conductor loss characteristic of CPW does not significantly impact the HBT DA design because the losses of the HBT device usually dominate the loss of the distributed transmission-line network [12].

A cascode HBT gain cell is used as a wide band gain block in the distributed amplifier design presented in this work. The cascode device is chosen because of its high frequency gain characteristics resulting from the elimination of Miller capacitance multiplication which effectively reduces the gain-bandwidth of conventional common-emitter based amplifiers. The schematic of the HBT cascode gain cell which is used in each section of the DA is given in Fig. 2. A common-emitter transistor, $Q_1$, is connected to a common-base transistor, $Q_2$, to form a cascode pair. Both $Q_1$ and $Q_2$ are $1 \times 4$ $\mu$m$^2$ single-emitter HBT's nominally biased at an $I_{ce} =$ mA and a $V_{ce} \approx 1.7$ V. Fig. 3(a) shows the $f_T$ and $f_{\max}$ performance of a $1 \times 4$ $\mu$m$^2$ HBT plotted versus collector current, Ice. This device achieves a peak $f_T$ and $f_{\max}$ of 46 GHz and 84 GHz, respectively. The size of the HBT device and operating current were chosen to maximize available gain and minimize input capacitance. Fig. 3(b) and (c) give the small-signal hybrid-$\pi$ model of the $1 \times 4$ $\mu$m$^2$ single-emitter HBT biased at an




(a)




(b)

**1 x 4 μm² HBT Hybrid-π Model Parameters**

| | | Fixed Parameters |
|---|---|---|
| Intrinsic Device | $B_{ac}$ | 27 |
| | $R_\pi$ (Ω) | 105 |
| | $C_\pi$ (ps) | 0.51 |
| | $\tau$(ps) | 0.54 |
| Distributed base and collector resistance | Rbx (Ω) | 16.1 |
| | Rbi (Ω) | 23.9 |
| | Rcx (Ω) | 1.8 |
| | Rci (Ω) | 2.2 |
| | Re (Ω) | 18.9 |
| Distributed collector-base capacitance | $C_{c1}$(fF) | 1 |
| | $C_{c2}$(fF) | 3 |
| Pad layout parasitics | Lb (pH) | 11 |
| | Lc (pH) | 23 |
| | Le (pH) | 1 |
| | Ccb (fF) | 23 |
| | Cce (fF) | 17 |
| | Cbe (fF) | 22 |
| Bias condition | $V_{ce}$ | 2 V |
| | $I_{ce}$ | 2m A |

(c)

Fig. 3. (a) $f_T$ and $f_{\max}$ versus Ic for a 1 × 4 $\mu$m$^2$ HBT device, (b) equivalent circuit hybrid-$\pi$ model, and (c) model parameters of the 1 × 4 $\mu$m$^2$ HBT device biased at an $I_{ce}$ = 2 mA and $V_{ce}$ = 2 V.

$I_{ce}$ = 2 mA and $V_{ce}$ = 2 V. At this bias, the HBT has an effective input capacitance of $C\pi \approx 0.5$ pF, a $\beta_{ac} \approx 28$, and an $f_{\max} \approx 75$ GHz.

Because of the large gain provided by the cascode cell, it is prone to being unstable. In order to maintain unconditional stability, the cascode cell employs negative feedback. In the cascode topology of Fig. 2, the base of transistor $Q_2$ is biased through a voltage divider provided by resistors $R_1$ and $R_{fb}$. This resistive bias network also provides substantial negative feedback at lower frequencies where the cascode topology is prone to oscillate. The base of $Q_2$ is also ac bypassed by a series $R$-$C$ network consisting of $C_{\text{bypass}}$ and $R_d$. This provides a modest amount of negative feedback at higher frequencies. The superior $G_{\max}$ performance of the HBT cascode cell compared to a conventional common-emitter HBT is illustrated in Fig. 4(a). Even with negative feedback, the cascode offers as much as *7 dB more available device gain* for frequencies above 20 GHz. The additional gain provided

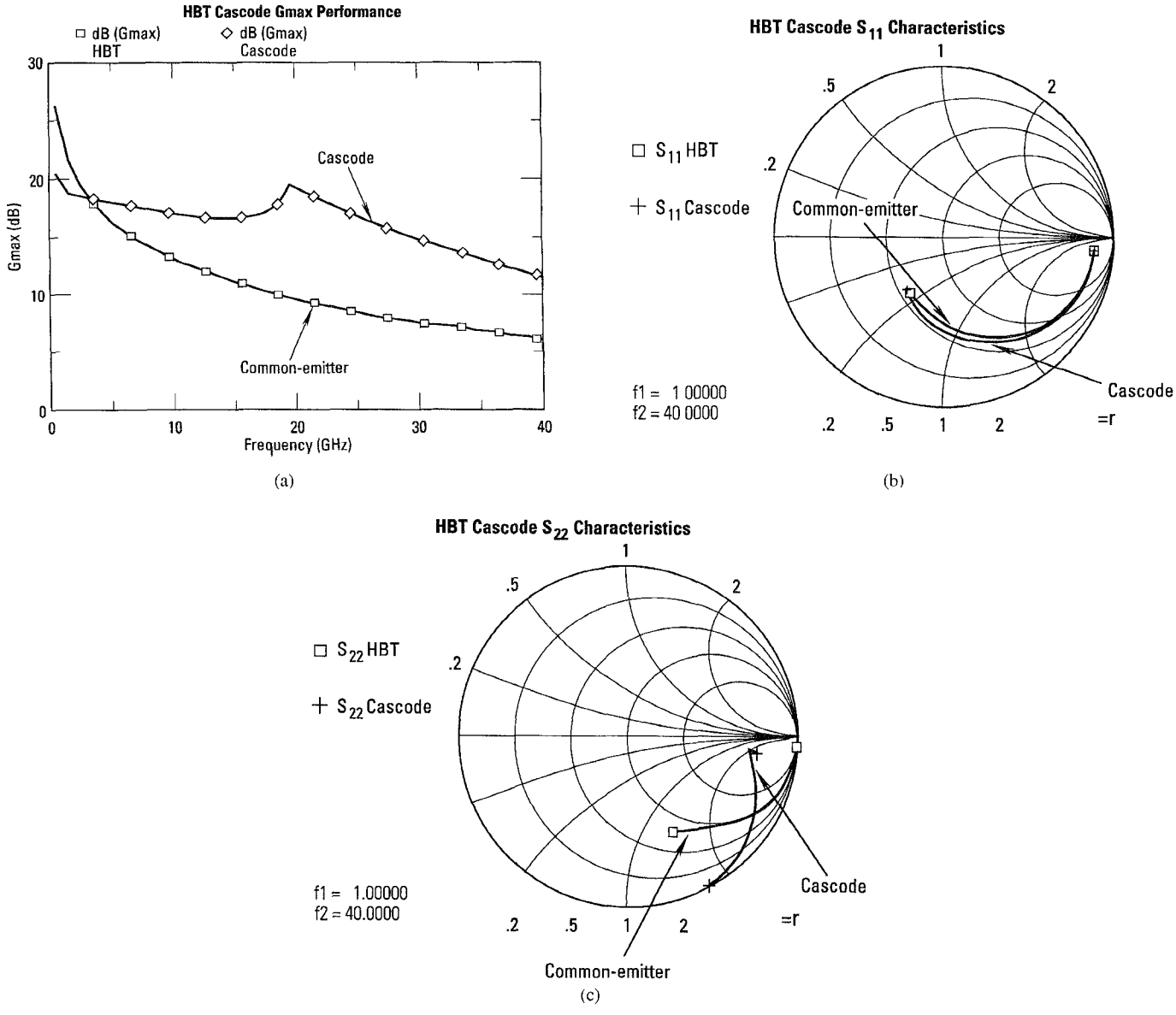



Fig. 4. (a) Gmax performance of the cascode cell compared to a conventional common-emitter HBT, and (b) $S_{11}$ of both the cascode and common-emitter, and c) $S_{22}$ of both cascode and common-emitter gain cells.

by the cascode enables the HBT DA to extend its bandwidth performance to 30 GHz. This results in an improvement of 35% in gain-bandwidth product over the conventional common-emitter HBT DA based on simulations.

The input and output scattering parameter characteristics, $S_{11}$ and $S_{22}$, of both cascode and common-emitter HBT gain cells are shown in Fig. 4(b) and (c). These Smith chart plots indicate that the input impedance of the cascode is similar to the common-emitter HBT; however, the output impedance of the cascode is less lossy than the conventional common-emitter. This is due to the increase in output impedance provided by the cascode which results in improved bandwidth performance of the output distributed transmission line.

A microphotograph of the fabricated CPW cascode HBT DA is shown in Fig. 5. The amplifier supply voltage is 5 V and draws 33 mA of current. The total dc power consumed by the MMIC is 165 mW. This microphotograph illustrates how compact the transmission line networks are about each of the 5 HBT cascode gain cells. Also shown is an enlarged view of one of the HBT cascode gain cells. Had a microstrip environment been used, a backside via would have been required for each of the cascode gain cells and would have made the input and output transmission-line networks almost physically impossible to layout. The microstrip design would have degraded the performance because of its sensitivity to proximity effects, whereas the CPW design geometrically confines the fields such that the proximity effects of adjacent structures are lessened. Recently reported experimental data supporting this claim have demonstrated as much as a 10 dB improvement in isolation between arms of a SPDT switch constructed using CPW compared to a microstrip approach [20]. Thus, our CPW DA approach allows the design to be more easily modeled without full EM analysis and results in a simple compact layout of $1.8 \times 1.2$ mm$^2$.

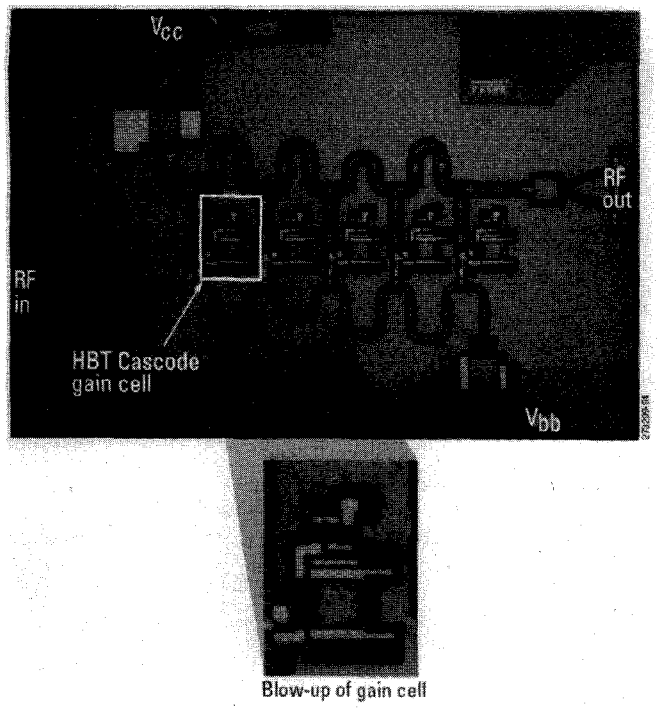



Fig. 5. Microphotograph of the fabricated CPW cascode HBT DA. Chip size is 1.8 × 1.2 mm$^2$.

## IV. Extending the Low Frequency Response Using HBT Active Loads

Distributed amplifiers are known for achieving high upper-band frequency performance by constructing artificial distributed transmission lines using the device's parasitic input and output capacitances. The DA topology results in bandwidths which often approach the device's $f_T$. However, most MMIC DA's are normally limited to a lower band edge of a few GHz. If the lower frequency limit can be extended, the distributed amplifier could be used for other applications such as ultra high data rate electro-optical communications as suggested in a recent work [7]. Currently, the low frequency limit is attributed to the dc blocking capacitors of the load terminations and the ac coupling capacitors at the input and output of the amplifier, both of which are often monolithically integrated using MIM capacitors. The input and output ac coupling capacitors in combination with the 50 Ω system impedance provide a high-pass pole whose frequency is given by $f_p = 1/(2\pi \cdot R_{\text{system}} \cdot C_{\text{coupling}})$. The dc blocking capacitors of the input and output load terminations also form a pole frequency below which the active load impedance increases resulting in increased gain and reduction in return-loss performance. In order to achieve lower frequency capability, large values of metal-insulator-metal (MIM) capacitors are required which may not be practical to realize on chip.

In order to extend the lower frequency response, the general practice is to integrate large value off-chip discrete capacitors. In some applications, the amplifier can be directly coupled requiring no capacitors at either the input or output of the amplifier. In this case, the integration of discrete off-chip capacitors are still required for the input and output transmission line load terminations in order to extend the lower frequency response. Often these discrete capacitors have self-resonances which fall within the passband of the amplifier. The problem may be compounded by the effects of wirebond parasitics in combination with the discrete capacitor components. These effects sometimes result in in-band resonances and gain ripple due to standing-waves in either of the input or output distributed transmission lines and are cumbersome to manage.

A convenient solution to extending the lower frequency response is to incorporate active loads to terminate the input and output transmission lines. Fig. 6 shows the proposed HBT active load terminations integrated with the HBT distributed amplifier discussed in the previous section. The active loads consist of an HBT common-collector device $(Q_{bb}, Q_{cc})$ which transforms a shunt load capacitance $(C_{bL}, C_{cL})$ on the base, to an effectively larger load capacitance when looking into the emitter. In this way an ac ground can be extended to lower frequencies using active HBT's without appreciably impacting chip size and yield. Fig. 7 conceptually illustrates the HBT active load impedance transformation. Fig. 7(a) gives the active load which is comprised of bypass capacitor $C_L$ whose impedance is transformed by HBT transistor $Q_T$. Resistor $R_{dc}$ is a base biasing resistor which is large than 1 KΩ and can be ignored in the ac analysis of the circuit. Resistor $R_L$ provides the resistive load termination in combination with the emitter resistance of the HBT device. The equivalent circuit and impedance, $Z_L(s)$, looking into the active load circuit is further illustrated in Fig. 7(b). This figure shows that the load impedance $Z_L(s)$ can be effectively modeled as a series $R$-$C$ network, where the $C$ is approximately equal to the load capacitance, $C_L$, times the low frequency beta, $\beta_o$, of transistor $Q_T$. The real part consists of the dynamic resistance of the device, $KT/(I_c \cdot q)$, in series with the emitter resistance, Re, external load resistor, $R_L$, and a base resistance term which is divided by the low frequency beta. The low frequency limit is determined by the pole frequency, $f_p = 1/(2\pi RC)$. The effective $R$ is constrained to $\approx$ 50 Ω which is the characteristic impedance of the distributed transmission lines. The capacitance is limited to values which are practical to integrate on a MMIC chip. The active load helps extend this limit by effectively multiplying the capacitance value $C_L$ of the monolithic capacitor by $\beta_o$. The low frequency ac beta $(\beta_o)$ of the device is dependent on the current density through the device. For the InGaAs HBT's of this work, the $\beta_o$ ranges from 15–35. This means that the low frequency limit of the HBT DA is improved by over an order of magnitude using this technique. For example, in order to realize 150 pF of capacitance, less than 10 pF of MIM capacitance needs to be integrated. This corresponds to a significant savings in area, not to mention an improvement in circuit yield which directly impacts cost.

The active HBT load termination was employed in the CPW cascode distributed amplifier design. Fig. 8 gives the simulated load impedances of the base and collector active load in comparison to conventional $R$-$C$ transmission line load terminations for a load capacitance $C_L = 10$ pF. This figure shows that the impedance of the conventional RC load is flat from 40 GHz down to 1 GHz, where the impedance ramps up very quickly. This is due to the 10 pF load capacitance.

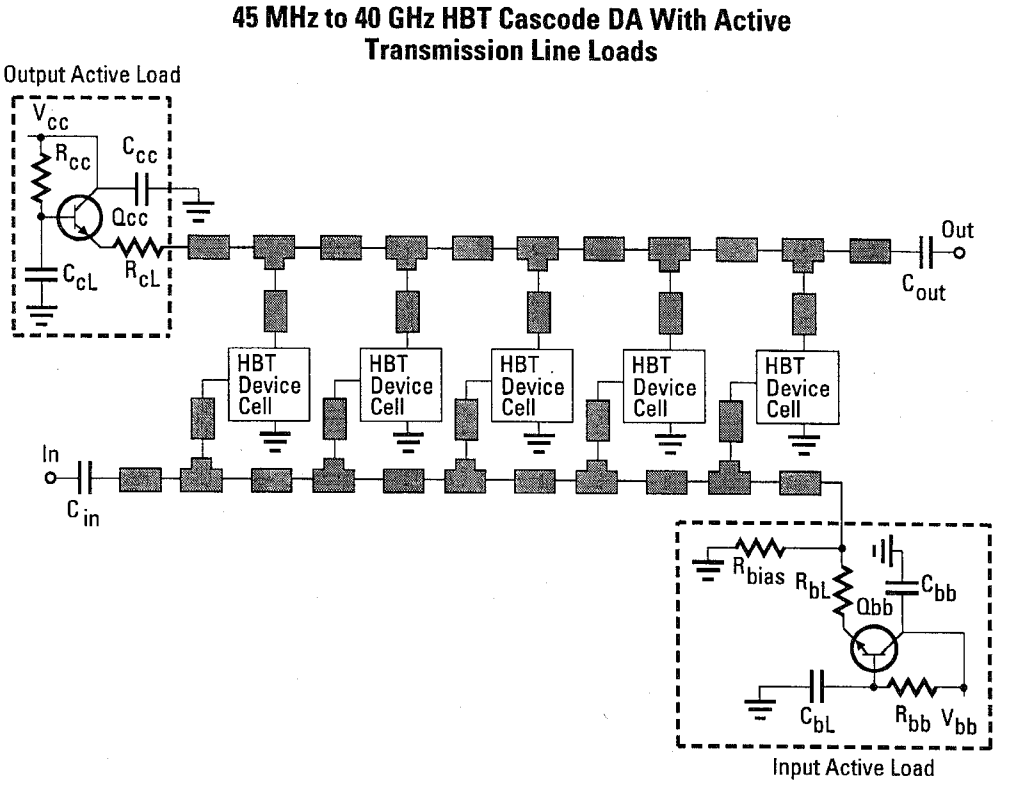



Fig. 6. HBT active load termination integrated with the HBT distributed amplifier.

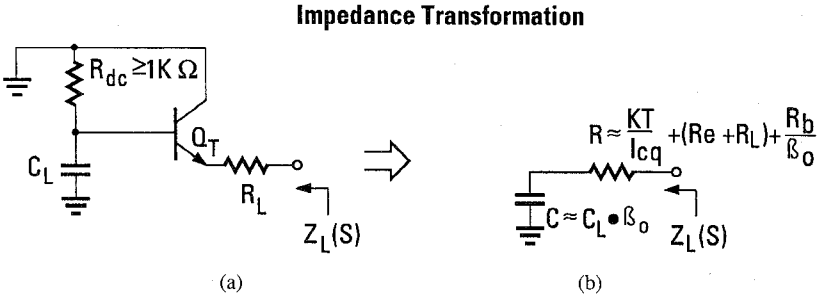



Fig. 7. (a) Active HBT transmission-line load termination. (b) Low frequency equivalent circuit model.

In comparison, the active HBT loads have impedances which are generally constant from 40 GHz down to 1 MHz. This illustrates the extended lower frequency response due to the load capacitance multiplication of the active load. Fig. 9 illustrates the HBT DA simulated performance for both active and passive load transmission line terminations. The gain of the passive $R$-$C$ terminated amplifier shows a pronounced gain ramping which occurs below 1 GHz. A corresponding abrupt degradation in return-loss also occurs at the same frequency for the passive $R$-$C$ terminated case. However, the gain of the actively terminated amplifier shows much less gain ramping at the lower frequencies and shows little or no effect on the low frequency return-loss performance. The actively terminated distributed amplifier demonstrates an improvement in gain and return-loss performance which significantly extends the useful frequency range of the amplifier.

A microphotograph of the fabricated actively terminated CPW HBT cascode five-section distributed amplifier is given in Fig. 10. Also shown is an enlarged view of the input HBT active load termination which integrates 1 HBT and a few resistors and metal-insulator-metal capacitors. The microphotograph of the HBT DA illustrates that the size of the MMIC is not significantly impacted by the integration of the active HBT load terminations, even though the low frequency performance is extended by a few decades in frequency.

## V. Measurements and Discussion

The original simulation performance of the HBT cascode CPW DA is compared against the measured performance as shown in Fig. 11. A 6.5 dB gain and 20 GHz 1-dB bandwidth was measured while a 5 dB gain and 25 GHz bandwidth was predicted. The measured return-losses are better than 13 dB across most of the 2–40 GHz band. The discrepancy between the original simulation and measured data is due to a difference in performance between the HBT design model and the actual fabricated devices. Because a cascode device is used for the

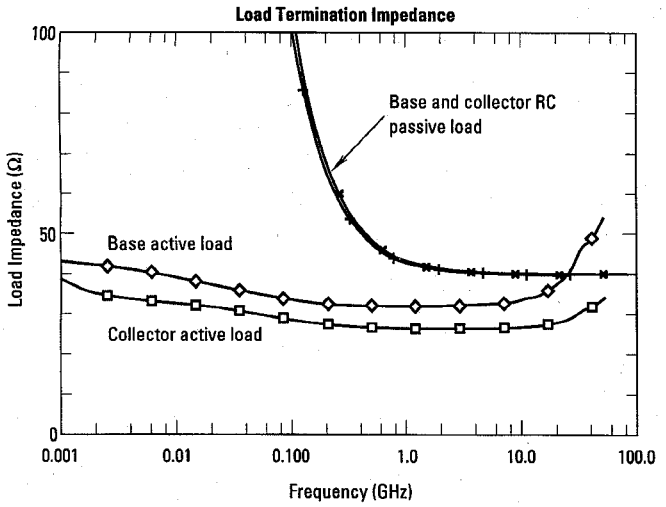



Fig. 8. Simulated load impedances of the base and collector active loads compared to the conventional passive $R$-$C$ load terminations for a load capacitance of $C_L = 10$ pF.

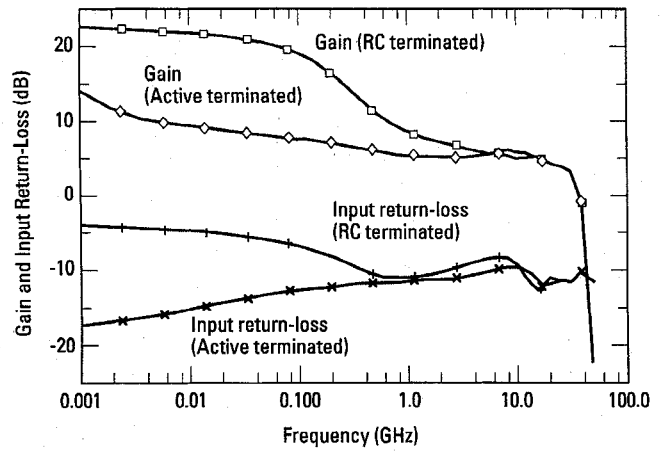



Fig. 9. Simulated effects of both active and passive transmission line load terminations on the HBT distributed amplifier performance.

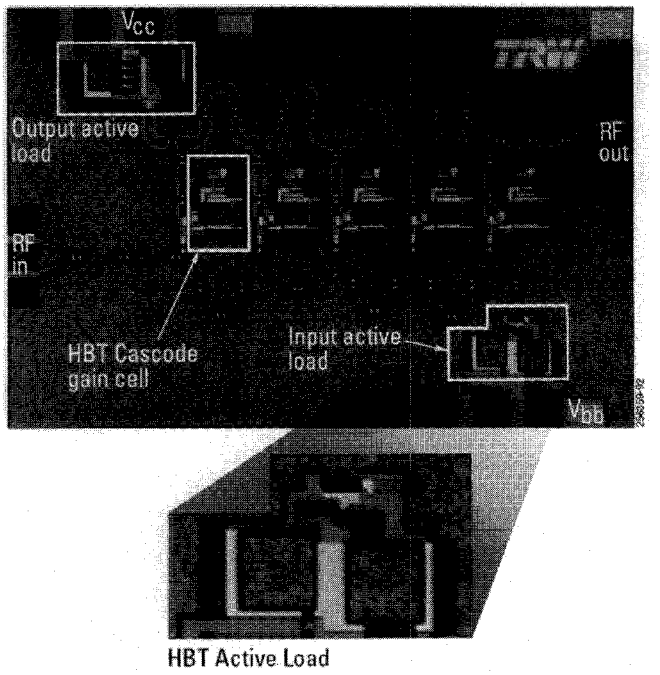



Fig. 10. Microphotograph of the fabricated actively terminated CPW HBT cascode five-section distributed amplifier.

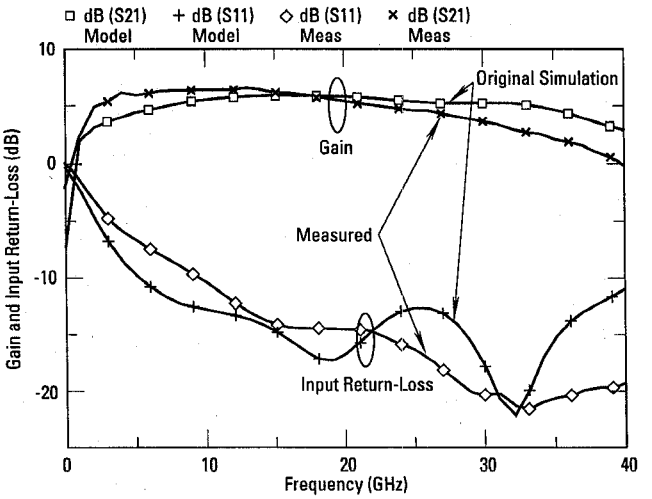



Fig. 11. Original simulation versus the measured performance.

gain cell, even a slight change in performance in the HBT's can result in a dramatic change in the amplifier's bandwidth response. When a new HBT design model is generated from the more recent device s-parameters (taken from the same site/wafer as the measured circuit data) and used in the simulation, the distributed amplifier simulated gain is within 0.5 dB of the measured gain for frequencies up to 40 GHz, shown in Fig. 12. The corresponding modeled input return-loss also tracks the measured data. For frequencies above 20 GHz, the input return-loss actually becomes much better than the modeled by >5 dB. Fig. 13 also illustrates that the modeled output return-loss tracks the measured data which is better than 15 dB across most of the band. Even the two resonances in the output return-loss response match to within a few GHz when comparing the modeled and measured response. Both Figs. 12 and 13 seem to reflect the accuracy of the LIBRA (4.0) CPW models when the circuit is layed-out to minimize proximity, radiation, and other parasitic effects.

Because the circuit simulation using the proper HBT device model closely matches the measured circuit performance, it is straightforward to redesign the amplifier to obtain improved bandwidth. The discrepancy between the original simulation and the measured data has been attributed to differences in the HBT device performance which is exaggerated by the cascode topology as mentioned above. Since the HBT DA performance has a gradual roll-off and seems to be very stable, the cascode feedback can be reduced to enhance the gain at the higher band edge. This is illustrated in Fig. 14 which shows the simulated gain and stability factor ($K$-factor) of the amplifier versus cascode feedback resistor, $R_{fb}$. At the nominal value of 300 Ω, the amplifier response has ≈ 22 GHz 1-dB BW and is unconditionally stable. For increasing values of $R_{fb}$, the upper band gain is significantly improved at the expense of stability ($K$-factor). An $R_{fb}$ of between 500–800 Ω will yield an unconditionally stable response with a 1-dB BW of ≈30–34

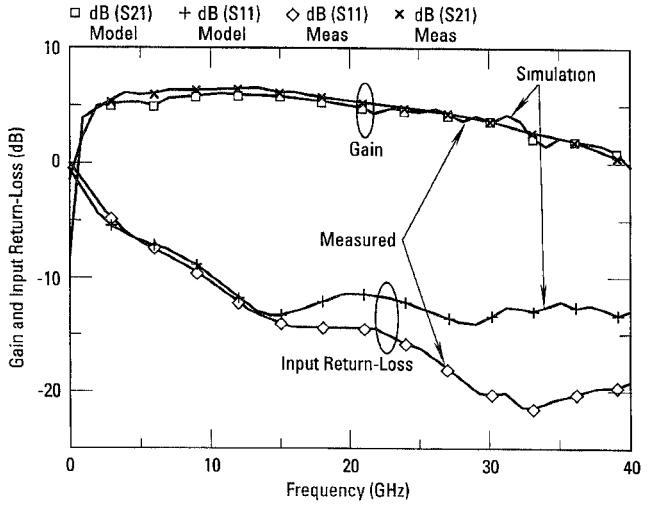



Fig. 12. Simulated gain and input return-loss using measured HBT $s$-parameters (from same wafer-site as the measured circuit) versus measured circuit performance.

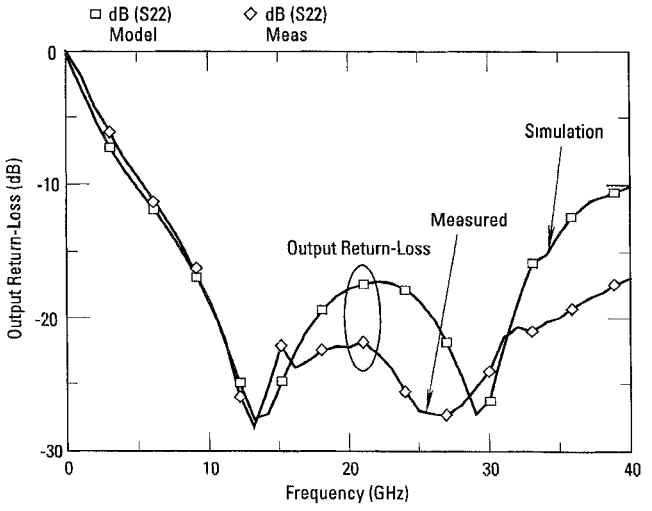



Fig. 13. Simulated output return-loss using measured HBT $s$-parameters (from same wafer-site as the measured circuit) versus measured circuit performance.

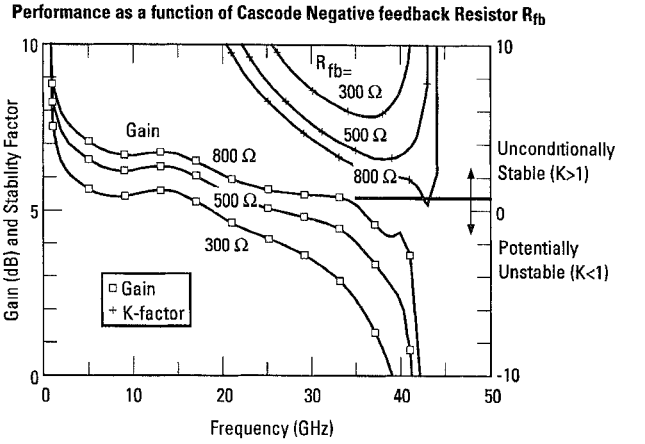



Fig. 14. Simulated gain and stability factor ($K$-factor) of the amplifier as a function of various cascode feedback resistors, $R_{fb}$ = 300 Ω, 500 Ω, and 800 Ω.

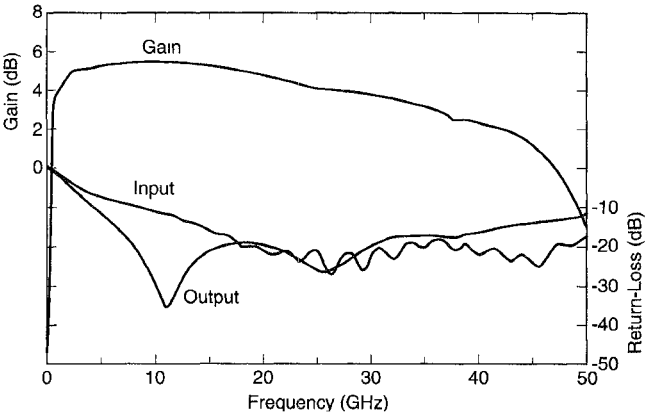



Fig. 15. Measured response of the redesigned HBT DA with an $R_{fb}$ = 600 Ω.

GHz. Fig. 15 shows the measured response of this redesigned HBT DA with an $R_{fb}$ = 600 Ω. The amplifier achieves a nominal gain of 5 dB and a bandwidth of 30 GHz which is close to the predicted bandwidth. This measured response is believed to represent the highest bandwidth so far reported for an HBT distributed amplifier. Furthermore, the redesigned DA's dc power consumption was reduced to only 125 mW through a 5 V supply.

In a separate demonstration, HBT active load terminations were integrated with the CPW DA in order to extend the lower band edge. Fig. 16 shows the low frequency performance of the actively terminated CPW HBT cascode amplifier. The upper frequency response above 3 GHz is similar to that obtained from the conventional RC terminated DA represented in Figs. 12 and 13 and is omitted in Fig. 16 in order to illustrate the detailed characteristics of the low frequency response. Fig. 16 shows a gain of 5 dB all the way down to 45 MHz where the gain begins to increase. The input return-loss is 12.5 dB at 3 GHz and begins to slowly degrade to <10 dB at the lower band edge. The output return-loss is better than 12.5 dB all the way down to 45 MHz. In comparison to the conventional $RC$ terminated DA discussed above, the active load terminations significantly extended the flat gain and good return-loss response by at least two decades in frequency at the lower band edge. During these measurements, there was no evidence of any instability or gain ripple across the 45 MHz–30 GHz band due to the employment of the active loads. The effects of the active load terminations on other parameters such as noise figure and $P_{1\,\mathrm{dB}}$ have not been characterized. The impact on these performance parameters will be heavily dependent on the bias of the active loads, and their design implementation.

The combination of the active load terminations with the CPW HBT cascode DA, results in an HBT distributed amplifier design topology which is capable of achieving baseband to millimeter-wave frequency performance. This demonstration shows promise for millimeter-wave HBT digital communication systems.

## VI. Conclusion

We have demonstrated a 2–30 GHz HBT distributed amplifier which is believed to be the highest reported bandwidth for

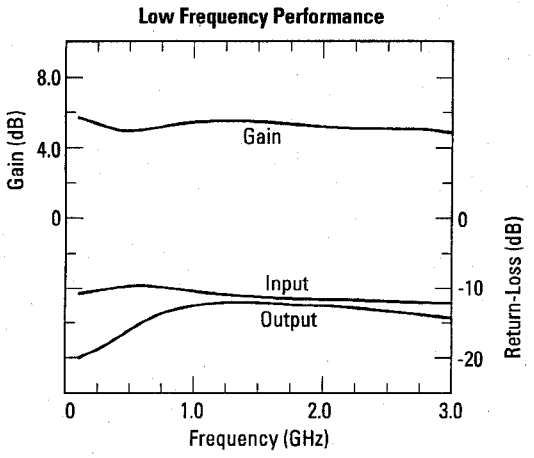



Fig. 16. Low frequency performance of the actively terminated CPW HBT cascode amplifier.

an HBT DA. A five-section cascode DA topology based on an InAlAs/InGaAs-InP HBT technology was used to achieve this benchmark. A CPW design environment was implemented in order to minimize interline coupling and proximity effects as well as to simplify the DA's fabrication. An HBT cascode with negative feedback was used to achieve the record upper band frequency response, while broadband active loads were used to extend MMIC performance below 45 MHz. The cascode InP-based HBT CPW DA demonstrates both design techniques and technology capability which can be applied to other millimeter-wave MMIC circuit functions such as active baluns for mixers, active combiners/dividers, and low dc power-broadband amplification at millimeter-wave frequencies.

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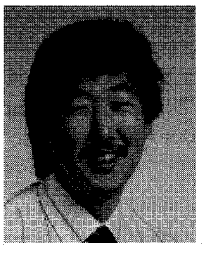


**Kevin W. Kobayashi** (M'93) received the BSEE degree from the University of California at San Diego in 1956, and the MSEE degree from the University of Southern California in 1991 under a TRW Fellowship.

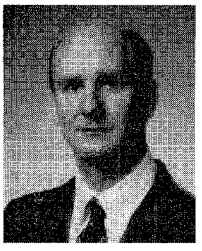
Since 1986 he has been working at TRW where he has been involved in the development of HBT, HEMT, and MESFET technologies. His primary focus has been in the design of HBT and HEMT MMIC's for insertion into TRW systems. He also provides design, consultation, and instruction for TRW's GaAs HBT Foundry, including several MMIC chip developments for standard and custom products for commercial wireless applications. His research activities have included the development of HBT low phase noise VCO's for synthesizers, broadband techniques for HBT amplifiers, active matching, and active feedback linearization techniques for power amplifiers, high linearity VGA's, and the design of low noise receivers and amplifiers. For the past few years, he has also been involved in the development of Complementary HBT and HEMT-HBT Selective MBE IC MMIC's.

**Liem T. Tran** (M'86) received the B.S. degree in applied physics from the California Institute of Technology and the M.S. degree in electrical engineering from the University of California at Berkeley.

He has been with TRW since 1988 working on GaAs and InP-based HBT advanced technology development.

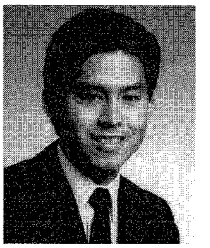
**John C. Cowles** (S'86–M'95) was born in São Paulo, Brazil, in 1965. He graduated *summa cum laude* with the B.S. degree in electrical engineering from the University of Pennsylvania, PA in 1987. He received the M.S. and Ph.D. degrees in 1989 and 1994, respectively, in electrical engineering from the University of Michigan, Ann Arbor.

In 1994, he joined the TRW RF Product Center, Redondo Beach, CA, where he is working currently on the fabrication and characterization of advanced GaAs and InP HBT technologies for MMIC's, analog and high-speed digital circuits.



**Thomas Ray Block** was born in St. Louis, MO, in 1962. He received the B.S. degree in electrical engineering from the University of Texas at Austin in May 1984. He received the M.S. degree in engineering in 1986 and the Ph.D. degree in engineering in 1991 from The University of Texas at Austin.

In 1991 he joined TRW as a Senior Member of Technical Staff engaged in molecular beam epitaxy growth of compound semiconductors for both research and production. He is involved in the growth of GaAs-based HBT's, HEMT's, and MESFET's and InP-based HBT's and HEMT's. In 1995 he became the Manager of the Advanced Materials Section at TRW.



**Aaron K. Oki** (M'85) was born in Honolulu, HI. He received the B.S. degree in electrical engineering in 1983 from the University of Hawaii, Manoa and the M.S. degree in electrical engineering and computer science in 1985 from the University of California, Berkeley.

Since joining TRW as a Member of the technical staff in 1985, he has been working on production and advanced development of HBT technology. In 1990, he became the Principle Investigator for HBT IR&D and Section Head of the HBT products section.

**Dwight C. Streit** (S'81–M'86–SM'92) received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1986.

He is currently Assistant Manager of the Microelectronics Product and Technology Development Department and Manager of the HEMT Technology Section in TRW's RF Products Center. He is Principal Investigator for several research and development projects related to III-V materials, monolithic HEMT-HBT integrated circuits, and quantum effect devices.